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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/499,720	02/08/2000	Dale C. Morris	10991915-1	1658

22879 7590 02/01/2005

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EXAMINER	
INOA, MIDYS	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 02/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/499,720	MORRIS ET AL.	
	Examiner	Art Unit	
	Midys Inoa	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 February 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The finality of the last office action, dated November 3rd, 2004 has been withdrawn in view of the new grounds of rejection set forth below.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Arora (6,393,556).

Regarding Claims 1 and 6, Arora discloses a method of promoting a current privilege level ("change current privilege level to a higher privilege level", Column 6, lines 46-61) wherein the current privilege level controls application instruction execution in the system by controlling accessibility to the system resources (Column 1, lines 30-41), the method comprising: performing a privilege level promotion instruction by the operating system (Column 4, lines 13-27, and Column 6, lines 46-61), the privilege promotion instruction being stored in a first page of memory not writable by application instructions at a first privilege level (privilege level stored in the architectural register set), the privilege promotion instruction including: reading a stored previous privilege level state; comparing the read previous privilege level state to the current privilege level (comparing the current privilege level to the instructions privilege level, column 6, lines 46-49); and if the previous privilege level state is equal to or less privileged than the current privilege level ("since the EPC instruction directs the processor to change the

architectural privilege level to a higher privilege level...", promoting the current privilege level to a second privilege level which is higher than the first privilege level ("...increase the architectural current privilege level from privilege level 3 to privilege level 0"). In comparing privilege levels, it is understood that the stored privilege level must be read in the comparison process.

Regarding Claims 12, 17 and 23 Arora discloses a computer system comprising a processor (Figure 2, processor 30) having current privilege level which controls accessibility to the system resources (Column 1, lines 30-41 and Column 4, lines 13-16; see Figure 2, CPL 38) and having a previous privilege level state ("second privilege level", Column 6, lines 27-32); a memory (Figure 2, Instruction memory 36) having a plurality of memory pages including a first memory page storing a privilege promotion instruction ("memory stores a plurality of instructions" such as an "EPC instruction which directs the processor to change the privilege level of the architectural current privilege level"; see Column 3, lines 20-25 and Column 4, lines 13-27) and not writable by application instructions at a first privilege level; and performing the privilege level promotion instruction as follows: reading a stored previous privilege level state; comparing the read previous privilege level state to the current privilege level (comparing the current privilege level to the instructions privilege level, column 6, lines 46-49); and if the previous privilege level state is equal to or less privileged than the current privilege level ("since the EPC instruction directs the processor to change the architectural privilege level to a higher privilege level...", promoting the current privilege level to a second privilege level which is higher than the first privilege level ("...increase the architectural current privilege level from

privilege level 3 to privilege level 0"). In comparing privilege levels, it is understood that the stored privilege level must be read in the comparison process.

Regarding Claims 2, 8, 13, and 19, Arora discloses the method of promoting a current privilege level wherein the step of performing the privilege promotion instruction further includes: if the previous privilege level state is more privileged then the current privilege level ("if the EPC instruction specifies a privilege level lower than or the same as the architectural current privilege level..."), taking an illegal operation fault ("the processor will issue a fault", Column 6, lines 55-61).

Regarding Claims 3, 9, 14, and 20, Arora discloses the method of promoting a current privilege level wherein the system resources include system registers (architectural register set, Column 3, lines 61-67).

Regarding Claims 4, 10, 15, and 21, Arora discloses the method of promoting a current privilege level wherein the system resources include system instructions ("memory 36 stores a plurality of instructions that are processed in the pipeline", column 3, lines 22-25).

Regarding Claims 5, 11, 16, and 22, Arora discloses the method of promoting a current privilege level wherein the system resources include memory pages (Figure 2, instruction memory 36).

Regarding Claim 7, 18, and 24 Arora discloses the method of promoting a current privilege level further comprising: performing a return instruction including: transferring instruction control flow to the stored return address to the first page of memory ("a return instruction would instruct the processor to decrease the architectural current privilege level to the

previous privilege level", Column 6, line 65-Column 7, line 3); and demoting the current privilege level to the stored previous privilege level.

Response to Arguments

3. Applicant's arguments with respect to claims 1-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Inoa whose telephone number is (571) 272-4207. The examiner can normally be reached on M-F 7:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Midys Inoa
Examiner
Art Unit 2188

MI

Mano Padmanabhan 7/31/05

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER